Amendments to the Claims:

Please amend claims 1, 2 and 10 as follows. Please cancel claim 6. This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A non-volatile semiconductor memory device comprising:

a substrate;

a charge storage region on the substrate;

a conductive region formed in a top portion of the substrate adjacent a sidewall of the charge storage region;

a control gate on the charge storage region;

a source electrode on the conductive region, wherein the source electrode is electrically isolated from the control gate by a source-side insulative spacer; and

a gate mask on the control gate, wherein the gate mask is in the shape of a spacer, the gate mask having a width that is substantially equal to a width of the underlying charge storage region and a width of the control gate, wherein the source electrode is of a height that is equal to or lower than a top of the gate mask ~~the gate mask operating as an etch mask during fabrication of the semiconductor memory device to define the underlying charge storage region and the control gate~~.

2. (currently amended) A non-volatile semiconductor memory device according to claim 1, further comprising:

a select gate formed on the substrate and a sidewall of the charge storage region ~~; and~~

~~a conductive region formed on the substrate adjacent another sidewall of the charge storage region~~, the charge storage region, the control gate, the gate mask and the select gate forming a first unit cell.

3. (original) A non-volatile semiconductor memory device according to claim 2 further comprising a second unit cell being symmetrical and opposite to the first unit cell, wherein the first unit and the second unit cell share the conductive region.

4. (original) A non-volatile semiconductor memory device according to claim 2, wherein the first unit cell further comprises a LDD spacer on a sidewall of the select gate.

5. (original) A non-volatile semiconductor memory device according to claim 2 further comprising:

a drain formed in the substrate adjacent to the select gate and opposite to the conductive region; and

a bit line electrode electrically connected to the drain.

6. (canceled)

7. (original) A non-volatile semiconductor memory device according to claim 2, wherein the select gate is in the shape of a spacer.

8. (original) A non-volatile semiconductor memory device according to claim 1, wherein the charge storage region comprises:

a floating gate dielectric layer on the substrate;

a floating gate on the floating gate dielectric layer; and

an inter poly dielectric layer on the floating gate.

9. (original) A non-volatile semiconductor memory device according to claim 1, wherein the charge storage region comprises an ONO layer.

10. (currently amended) A non-volatile semiconductor memory device comprising:

a substrate having a source and a drain;

a channel between the source and the drain;

a charge storage region over the channel;

a control gate over the charge storage region;

a gate mask ~~being formed~~ on an entire top surface of the control gate and being in the shape of a spacer , the gate mask having a width that is substantially equal to a width of the underlying charge storage region and a width of the control gate; and

a select gate on the channel and between the charge storage region and the drain; the charge storage region, the channel, the drain, the control gate and the select gate forming a first unit cell.

11. (original) A non-volatile semiconductor memory device according to claim 10 further comprising a second unit cell being symmetrical and opposite to the first unit cell, wherein the first unit and the second unit cell share the source.

12. (original) A non-volatile semiconductor memory device according to claim 10, wherein the select gate is in the shape of a spacer.

13. (canceled)

14. (original) A non-volatile semiconductor memory device according to claim 10 further comprising a LDD spacer on a sidewall of the select gate.

15. (original) A non-volatile semiconductor memory device according to claim 10 further comprising:

a bit line electrode connected to the drain; and

a source electrode on the source, wherein the source electrode is electrically isolated

from the control gate by a source-side spacer.

16. (original) A non-volatile semiconductor memory device according to claim 10, wherein the charge storage region comprises:

a floating gate dielectric layer on the substrate;

a floating gate on the floating gate dielectric layer; and

an inter poly dielectric layer on the floating gate.

17. (original) A non-volatile semiconductor memory device according to claim 10, wherein the charge storage region comprises an ONO layer.